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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,607	12/29/2003	James S. Song	TI-35767 (032350.B545)	8925

23494 7590 05/08/2006

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 05/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,607	SONG ET AL.	
	Examiner	Art Unit	
	James Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-12 are rejected under 35 U.S.C. 102(e) as being highly anticipated by Wang et al. (U.S. Patent No. 6,549,045 B1) (hereinafter referred to as Wang).

As to claim 1, Wang discloses a delay equalizer (clock channel 20) for balancing clock signals in a clock tree (Wang discloses a clock system wherein said system provides multiple clocks with low skew and proper alignment; column 2, lines 5-15 and column 4, lines 17-21), comprising: a register (flip-flop 110) operable to: receive (as shown in figure 2) a divided input clock signal (105) (Wang discloses the flip-flop [110] receiving M-bit clock signals provided from a bit string within a shift register [100] thus producing a divided frequency; column 2, lines 35-43 and column 4, lines 40-58 and column 5, lines 52-63 and column 6, lines 40-44); receive (as shown in figure 2) a non-divided input clock signal (Wang discloses the flip-flop [110] receiving an undivided input clock signal [50] to drive the flip-flop; column 4, lines 40-58); and generate a first output clock signal (115) based on the received divided input clock signal (105) and the received non-divided input clock signal (50), the first output clock signal being associated with a first delay (Wang discloses the flip-flop [110] receiving signals 50 and 105

through a delay [D-type] flip-flop and thus producing a delayed output signal [115] that is delayed secondary to the propagation of the signals through the flip-flop; column 4, lines 47-58 and column 5, lines 19-23); a delay line (delay circuit 120) operable to: receive (as shown in figure 2) the non-divided input clock signal (50) (column 4, lines 63-67); delay the non-divided input clock signal for a time substantially equivalent to the first delay associated with the first output clock signal (Wang discloses the signals produced by 110 and 120 [signals 115 and 125] being matched and therefore having equal delays; column 5, lines 14-30); and generate a second output clock signal (125) being associated with a second delay substantially equal to the first delay of the first output signal (column 4, lines 63-67 and column 5, lines 14-30); and a multiplexer (multiplexer circuit 130) operable to: receive (as shown in figure 2) the first output clock signal (115) and the second output clock signal (125) (column 5, lines 1-3); receive (as shown in figure 2) a select control signal (MUXADR signal) indicating which of the first output clock signal or the second output clock signal to select (column 5, lines 4-13); select either the received first output clock signal (115) or the second output clock signal (125) based on the select control signal (column 5, lines 4-13); and generate the selected first output clock signal (115) or second output clock signal (125) as a substantially balanced third output clock signal (output 135) (Wang discloses the output signal from the multiplexer [130] being a matched signal since the inputs to the multiplexer are matched and therefore balanced; column 5, lines 1-7 and column 5, lines 19-30 and column 8, line 53 thru column 9, line 13).

As to claim 2, Wang discloses the delay equalizer wherein: the divided clock in signal being associated with a functional mode (channel) of a device (10) comprising the delay equalizer (Wang discloses clock output signals being selectable parameters within the circuit

utilizing the divided/undivided clock balancing scheme; column 4, lines 7-39); and the select control signal (MUXADR) received by the multiplexer (130) comprises a divided/non-divided select control signal (column 5, lines 4-13); the delay equalizer (20) is operable to substantially balance the input clock signal between one or more functional modes of the device (Wang discloses all of the possible output paths being matched with minimal skew and therefore balanced; column 4, lines 33-39).

As to claim 3, Wang discloses the delay equalizer wherein the delay equalizer is implemented at the output of existing clock dividing and selection logic (Wang discloses the divided/undivided clock signals being drive by an input clock [50] and clock selection bits [40-1 thru 40-N] inputs at the circuit [10]; column 4, lines 7-32).

As to claim 4, Wang discloses the delay equalizer wherein the delay equalizer is implemented within existing clock dividing and selection logic, the clock dividing and selection logic being redesigned to include the delay equalizer (As is known in the art, cascading clock division schemes can be selected in a clock tree synthesis method to balance the clocks within an entire system that are needed for different devices; column 1, line 26 thru column 2, line 2).

As to claim 5, Wang discloses the delay equalizer wherein the delay equalizer is associated with a clock-gating cell and is operable to provide the substantially balanced third output clock signal to the clock-gating cell as an input clock signal to the clock-gating cell such that an output clock signal generated by the clock-gating cell is substantially balanced (As is known in the art, a clock tree synthesis tool can be applied to balance all the clocks throughout the system and therefore necessitates clock gates to select a desired clock, whether divided or

undivided, dependent on control signals used by said synthesizers; column 1, line 26 thru column 2, line 2).

As to claim 6, Wang discloses the delay equalizer wherein: the register comprises a flip-flop register (110) (column 4, lines 40-44); and the delay line (120) comprises one or more buffers for delaying the non-divided clock signal (Wang discloses the delay circuit in comprising inverter buffers [305, 310, 330 and 335]; column 8, lines 53-63).

As to claim 7, Wang discloses a method for balancing clock signals in a node (channel) of a clock tree (column 2, lines 5-34), comprising: receiving a divided input clock signal (via signal 105 from shift register 100) at a register (flip-flop 110) (Wang discloses the flip-flop [110] receiving M-bit clock signals provided from a bit string within a shift register [100] thus producing a divided frequency; column 2, lines 35-43 and column 4, lines 40-58 and column 5, lines 52-63 and column 6, lines 40-44); receiving a non-divided input clock signal (via signal 50) at the register (flip-flop 110) (Wang discloses the flip-flop [110] receiving an undivided input clock signal [50] to drive the flip-flop; column 4, lines 40-58); generating at the register (via signal 115) a first output clock signal based on the received divided input clock signal (105) and the received non-divided input clock signal (50), the first output clock signal (115) being associated with a first delay (Wang discloses the flip-flop [110] receiving signals 50 and 105 through a delay [D-type] flip-flop and thus producing a delayed output signal [115] that is delayed secondary to the propagation of the signals through the flip-flop; column 4, lines 47-58 and column 5, lines 19-23); receiving the non-divided input clock signal (50) at a delay line (delay circuit 120) (column 4, lines 63-67); delaying at the delay line the non-divided input clock signal for a time substantially equivalent to the first delay associated with the first output clock

signal (Wang discloses the signals produced by 110 and 120 [signals 115 and 125] being matched and therefore having equal delays; column 5, lines 14-30); generating at the delay line (120) a second output clock signal (120) being associated with a second delay substantially equal to the first delay of the first output signal (Wang discloses the signals produced by 110 and 120 [signals 115 and 125] being matched and therefore having equal delays; column 5, lines 14-30); receiving at a multiplexer (130) the first output clock signal (via signal 115) and the second output clock signal (via signal 125) (column 5, lines 1-3); receiving at the multiplexer a select control signal (MUXADR signal) indicating which of the first output clock signal or the second output clock signal to select (column 5, lines 4-13); selecting at the multiplexer either the received first output clock signal (115) or the second output clock signal (125) based on the select control signal (MUXADR signal) (column 5, lines 4-13); and generating the selected first output clock signal (115) or second output clock signal (125) as a substantially balanced third output clock signal (output 135) (Wang discloses the output signal from the multiplexer [130] being a matched signal since the inputs to the multiplexer are matched and therefore balanced; column 5, lines 1-7 and column 5, lines 19-30 and column 8, line 53 thru column 9, line 13).

As to claim 8, Wang discloses the method wherein: the divided clock in signal being associated with a functional mode (channel) of a device (10) comprising the delay equalizer (Wang discloses clock output signals being selectable parameters within the circuit utilizing the divided/undivided clock balancing scheme; column 4, lines 7-39); and the select control signal (MUXADR) received by the multiplexer (130) comprises a divided/non-divided select control signal (column 5, lines 4-13); the method substantially balancing the input clock signal between

one or more functional modes of the device (Wang discloses all of the possible output paths being matched with minimal skew and therefore balanced; column 4, lines 33-39).

As to claim 9, Wang discloses the method wherein the method is performed on the output of existing clock dividing and selection logic (Wang discloses the divided/undivided clock signals being drive by an input clock [50] and clock selection bits [40-1 thru 40-N] inputs at the circuit [10]; column 4, lines 7-32).

As to claim 10, Wang discloses the method wherein the method is integrated into existing clock dividing and selection logic, the clock dividing and selection logic having been redesigned for implementing the method (As is known in the art, cascading clock division schemes can be selected in a clock tree synthesis method to balance the clocks within an entire system that are needed for different devices; column 1, line 26 thru column 2, line 2).

As to claim 11, Wang discloses the method further comprising providing the substantially balanced third output clock signal to a clock-gating cell as an input clock signal to the clock-gating cell such that an output clock signal generated by the clock-gating cell is substantially balanced (As is known in the art, a clock tree synthesis tool can be applied to balance all the clocks throughout the system and therefore necessitates clock gates to select a desired clock, whether divided or undivided, dependent on control signals used by said synthesizers; column 1, line 26 thru column 2, line 2).

As to claim 12, Wang discloses the method wherein: the register comprises a flip-flop register (110) (column 4, lines 40-44); and the delay line comprises one or more buffers for delaying the non-divided clock signal (Wang discloses the delay circuit in comprising inverter buffers [305, 310, 330 and 335]; column 8, lines 53-63).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (U.S. Patent Publication No. 2003/0135836 A1) (hereinafter referred to as Chang) in view of Wang et al. (U.S. Patent No. 6,549,045 B1) (hereinafter referred to as Wang).

As to claim 13, Chang discloses a method for balancing one or more clock signals in a clock tree (38 of figure 8) having a multi-mode (multiple levels) clock distribution (paragraphs 19 and 20), comprising: associating a first delay equalizer (adding buffers 48 and 49 to delay signals) with at least one of a plurality of clock-gating cells (gates 50-52 or any number thereof) arranged in one or more levels in the clock tree, the first delay equalizer operable to provide a balanced input clock signal to the clock-gating cell (Chang also discloses the clock tree synthesis [CTS] tool balancing the tree and subtrees dependent on the clock tree's specific gating scheme; paragraphs 36-39 and 42-43) such that an output clock signal generated by the clock-gating cell is substantially balanced (Chang discloses a gated clock tree system [38] which is capable of comprising any number of gates [50-52] to distribute balanced clock signals to respective subtrees and sinks [40-47] to deliver balanced clock signals; paragraphs 36-39); extracting a common clock distribution topology (path) from the clock tree, the topology accounting for substantially all of modes (low levels and high levels) paths of the topology (Chang discloses a

clock tree synthesis [hereinafter referred to as CTS] tool extracts [synthesizes] all lower level trees and works upward in the tree hierarchy until the entire clock tree is balanced; paragraph 39); determining one or more clock paths (subtrees) to be balanced, each comprising a multi-mode dependant clock path (Chang discloses determining which subtree paths need to be re-evaluated in order to properly balance the entire tree; paragraphs 43); analyzing any local clock paths that were left out of the common clock distribution topology (Chang discloses creating new endpoints in the clock subtree structures to properly evaluate and determine a balanced subtree by inserting new buffers to balance the delays; if the subtree is not balanced, a new endpoint is determined thus re-evaluated thus discovering new subtree branches that were left out of the evaluation process before; paragraphs 44-45); developing a local balancing strategy (subtree synthesis) for the local clock paths that were left out of the common clock distribution topology to determine one or more constraints for substantially balancing the local clock paths (Chang discloses balancing the lower subtrees and combining [synthesizing] all of the subtrees using two techniques [zero-skew algorithm and subtree compression process] and re-evaluating until all subtrees are balanced; paragraphs 52-54); combining (synthesizing) the local balancing strategy (subtree analysis) with the common clock distribution (starting at the lower levels and working upward to all levels of the tree) to form a clock tree synthesis constraint to substantially balance the common clock distribution topology and the local clock paths in a substantially automatic process (Chang discloses balancing all levels of the tree using the CTS algorithm that automatically loops through a balancing/synthesizing process until the entire tree is synthesized; paragraphs 47-50).

Chang fails to disclose associating a second delay equalizer with each of one or more clock-dividing and selection modules in the clock tree, the second delay equalizer operable to substantially balance the one or more clock signals between one or more functional modes until the entire clock tree is balanced to include the clock-dividing paths of the modes.

Wang teaches a clock distribution system (200) comprising one or more second delay equalizers (220-1 and 220-2 or more as depicted in figure 1 via clock channels 40-1 thru 40-N; column 4, lines 17-21) each associated with each of one or more clock-dividing (in combination with flip-flops [110-1 and 110-2] and shift registers [100-1 and 110-2]; column 5, lines 52-63 and column 6, lines 40-44) and selection modules (multiplexers 130-1 and 130-2) in the clock system, each second delay equalizer operable to substantially balance the one or more clock signals (Wang discloses the output signal from the multiplexers [130] being a matched signal since the inputs to the multiplexer are matched and therefore balanced; column 5, lines 1-7 and column 5, lines 19-30 and column 8, line 53 thru column 9, line 13). Wang also has the added feature of delivering an unbalanced divided signal from the shift registers (100 via signal 105) that has a phase difference of ½ cycle if desired (column 6, lines 40-52).

It would have been obvious to one of ordinary skill of the art having the teachings of Chang and Wang at the time the invention was made, to modify the gated clock tree of Chang to include balanced frequency divided clock signals from delay elements as taught by Wang such that balanced frequency divided signals are delivered between one or more functional modes as done so with delayed clock signals of the clock tree and including said divided clock paths within the clock balancing and synthesizing methods. One of ordinary skill in the art would be motivated to make this combination of including balanced frequency divided clock signals

between multiple levels and including these divided clocks within the clock balancing and synthesizing methods in view of the teachings of Wang, as doing so would give the added benefit of delivering an unbalanced divided signal from the shift registers (100 via signal 105) that has a phase difference of ½ cycle if desired (column 6, lines 40-52).

As to claim 14, Chang discloses the method wherein determining the one or more clock paths to be balanced comprises: determining an impact that balancing a particular clock path (subtree) would have on overall clock tree balance and performance of a device associated with the clock tree (Chang discloses the CTS tool determining how a low level subtrees that have been balanced would affect the overall tree while synthesizing; paragraph 39); determining whether the determined impact of the particular clock path exceeds a predetermined impact (Chang discloses the CTS tool determining if a particular path [subtree] exceeds a predetermined impact [path delays varying widely]; paragraph 45); and if it is determined that the determined impact of balancing the particular clock path exceeds the predetermined impact, determining that the particular clock path should be balanced (Chang discloses the CTS tool repeating the process until a subtree is balanced; paragraph 45).

As to claim 15, Chang discloses the method wherein determining an impact that balancing the particular clock path would have on the overall clock tree comprises: determining whether the particular clock path operates asynchronously to other portions of the clock tree (Chang discloses the clocked devices processing the data can be comprised of registers and flip-flops, as is known in the art, can be synchronous or asynchronous which therefore would necessitate evaluation of asynchronous devices being present; paragraph 36); and if so, concluding that the impact of balancing the particular clock path does not exceed the

predetermined impact (Chang discloses the CTS tool ensuring all signals occur synchronously and therefore evaluating if said process has an impact on the timing; paragraph 36).

As to claim 16, Chang discloses the method further comprising inserting one or more exclusive-NOR (XNOR) gates throughout the clock tree to balance one or more portions of the clock tree, each XNOR gate (Chang discloses the CTS tool inserting additional buffers, as is known in the art, can comprise XNOR gates; paragraph 37) operable to: receive an input clock signal on an input clock path (Chang discloses the clock paths within figure 8 comprising input clock signals into the buffers along the clock paths; paragraphs 36 and 37); receive a test mode signal on a test mode path (paragraph 14); and generate an output clock signal on an output clock path based on an XNOR operation, a delay from the input clock path to the output clock path being independent of a delay from the test mode path to the output clock path (Chang discloses buffers being added to alter delays for clock balancing wherein the gates are controlled to select the path desired dependent on the synthesis process; paragraphs 41-45).

As to claim 17, Chang discloses the method wherein when the test mode signal received on the test mode path asserts test mode, the output clock signal generated by the XNOR gate comprises a non-inverted output clock signal (Chang discloses ensuring all signals occur synchronously and therefore ensuring no signals are inverted; paragraphs 3-7 and 36).

As to claim 18, Chang discloses a system for balancing one or more clock signals in a clock tree having a multi-mode (multiple levels) clock distribution (paragraphs 19 and 20), comprising: one or more first delay equalizers (buffers 48 and 49 to delay signals) each associated with at least one of a plurality of clock-gating cells (gates 50-52 or any number thereof) arranged in one or more levels (lower levels and upper levels) in the clock tree (38 in

figure 8), each first delay equalizer (buffers) operable to provide a balanced input clock signal to the clock-gating cell such that an output clock signal generated by the clock-gating cell is substantially balanced (Chang also discloses the clock tree synthesis [CTS] tool balancing the tree and subtrees dependent on the clock tree's specific gating scheme; paragraph 43) wherein the first equalizers substantially balance the one or more clock signals in the clock tree (Chang discloses a gated clock tree system [38] which is capable of comprising any number of gates [50-52] to distribute balanced clock signals to respective subtrees and sinks [40-47] to deliver balanced clock signals; paragraphs 36-39).

Chang fails to disclose one or more second delay equalizers each associated with each of one or more clock-dividing and selection modules in the clock tree, each second delay equalizer operable to substantially balance the one or more clock signals between one or more functional modes wherein the second equalizers substantially balance the one or more clock signals in the clock tree.

Wang teaches a clock distribution system (200) comprising one or more second delay equalizers (220-1 and 220-2 or more as depicted in figure 1 via clock channels 40-1 thru 40-N; column 4, lines 17-21) each associated with each of one or more clock-dividing (in combination with flip-flops [110-1 and 110-2] and shift registers [100-1 and 110-2]; column 5, lines 52-63 and column 6, lines 40-44) and selection modules (multiplexers 130-1 and 130-2) in the clock system, each second delay equalizer operable to substantially balance the one or more clock signals (Wang discloses the output signal from the multiplexers [130] being a matched signal since the inputs to the multiplexer are matched and therefore balanced; column 5, lines 1-7 and column 5, lines 19-30 and column 8, line 53 thru column 9, line 13). Wang also has the added

feature of delivering an unbalanced divided signal from the shift registers (100 via signal 105) that has a phase difference of ½ cycle if desired (column 6, lines 40-52).

It would have been obvious to one of ordinary skill of the art having the teachings of Chang and Wang at the time the invention was made, to modify the gated clock tree of Chang to include balanced frequency divided clock signals from delay elements as taught by Wang such that balanced frequency divided signals are delivered between one or more functional modes as done so with delayed clock signals of the clock tree of Chang. One of ordinary skill in the art would be motivated to make this combination of including balanced frequency divided clock signals between multiple levels in view of the teachings of Wang, as doing so would give the added benefit of delivering an unbalanced divided signal from the shift registers (100 via signal 105) that has a phase difference of ½ cycle if desired (column 6, lines 40-52).

As to claim 19, Chang discloses the system further comprising one or more exclusive-NOR (XNOR) gates inserted throughout the clock tree (Chang discloses the CTS tool inserting additional buffers, as is known in the art, can comprise XNOR gates; paragraph 37) to balance one or more portions of the clock tree, each XNOR gate operable to: receive an input clock signal on an input clock path; receive a test mode signal on a test mode path (Chang discloses the clock paths within figure 8 comprising input clock signals into the buffers along the clock paths; paragraphs 36 and 37); and generate an output clock signal on an output clock path based on an XNOR operation, a delay from the input clock path to the output clock path being independent of a delay from the test mode path to the output clock path (Chang discloses buffers being added to alter delays for clock balancing wherein the gates are controlled to select the path desired dependent on the synthesis process; paragraphs 41-45).

As to claim 20, Chang discloses the system wherein when the test mode signal received on the test mode path asserts test mode, the output clock signal generated by the XNOR gate comprises a non-inverted output clock signal (Chang discloses ensuring all signals occur synchronously and therefore ensuring no signals are inverted; paragraphs 3-7 and 36).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

James Sugent
Patent Examiner, Art Unit 2116
April 27, 2006